CSE460: VLSI Design

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Section- 07

Lab Assignment 5

General guidelines

Draw the circuit using the appropriate tool as taught in the lab and rectify all design errors (if

any), submit the full screen screenshots of the design file and the simulation file **with proper**

**discussion.**

**Problem:**

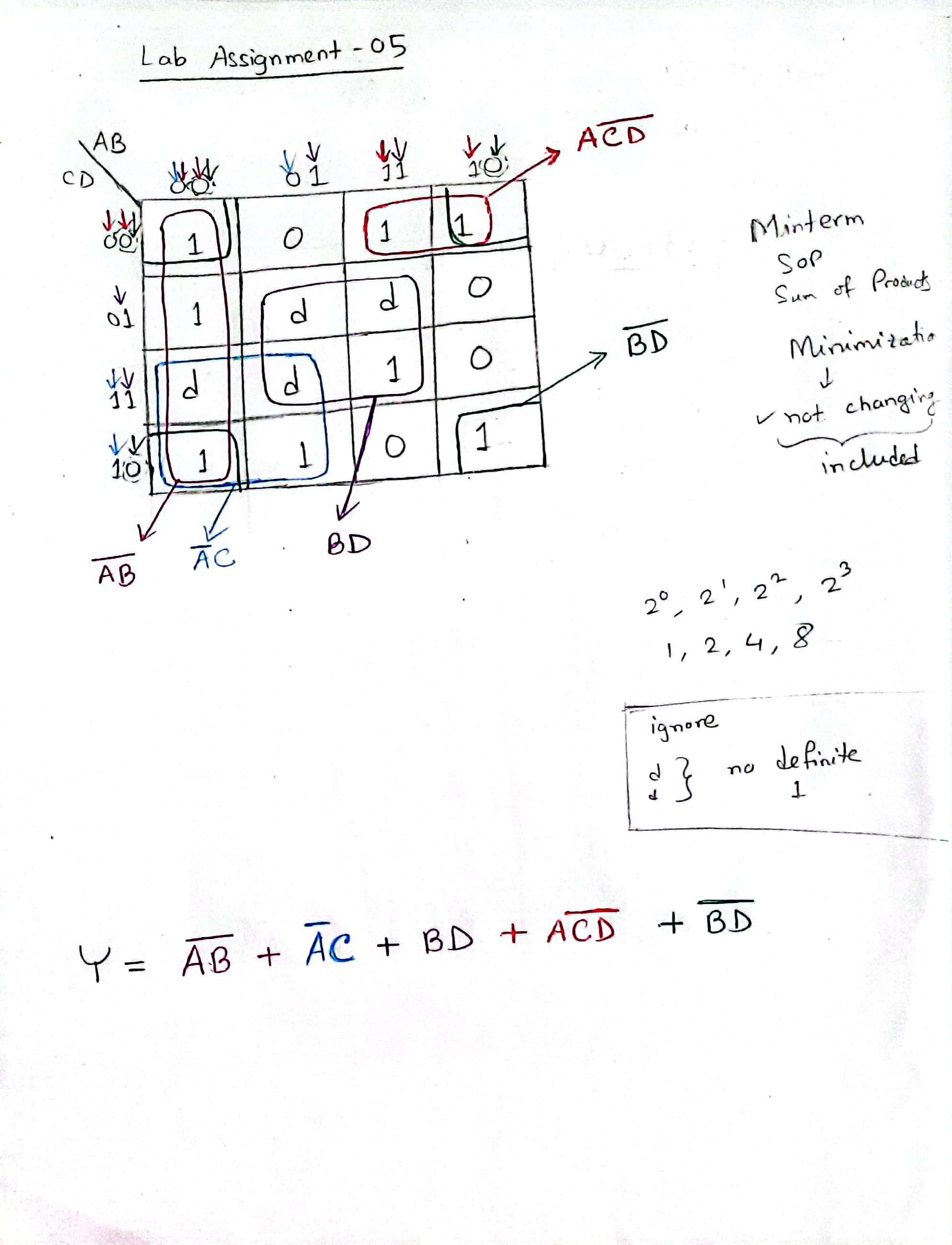
Derive the Boolean logic expression from the following K-Map and implement the logic function

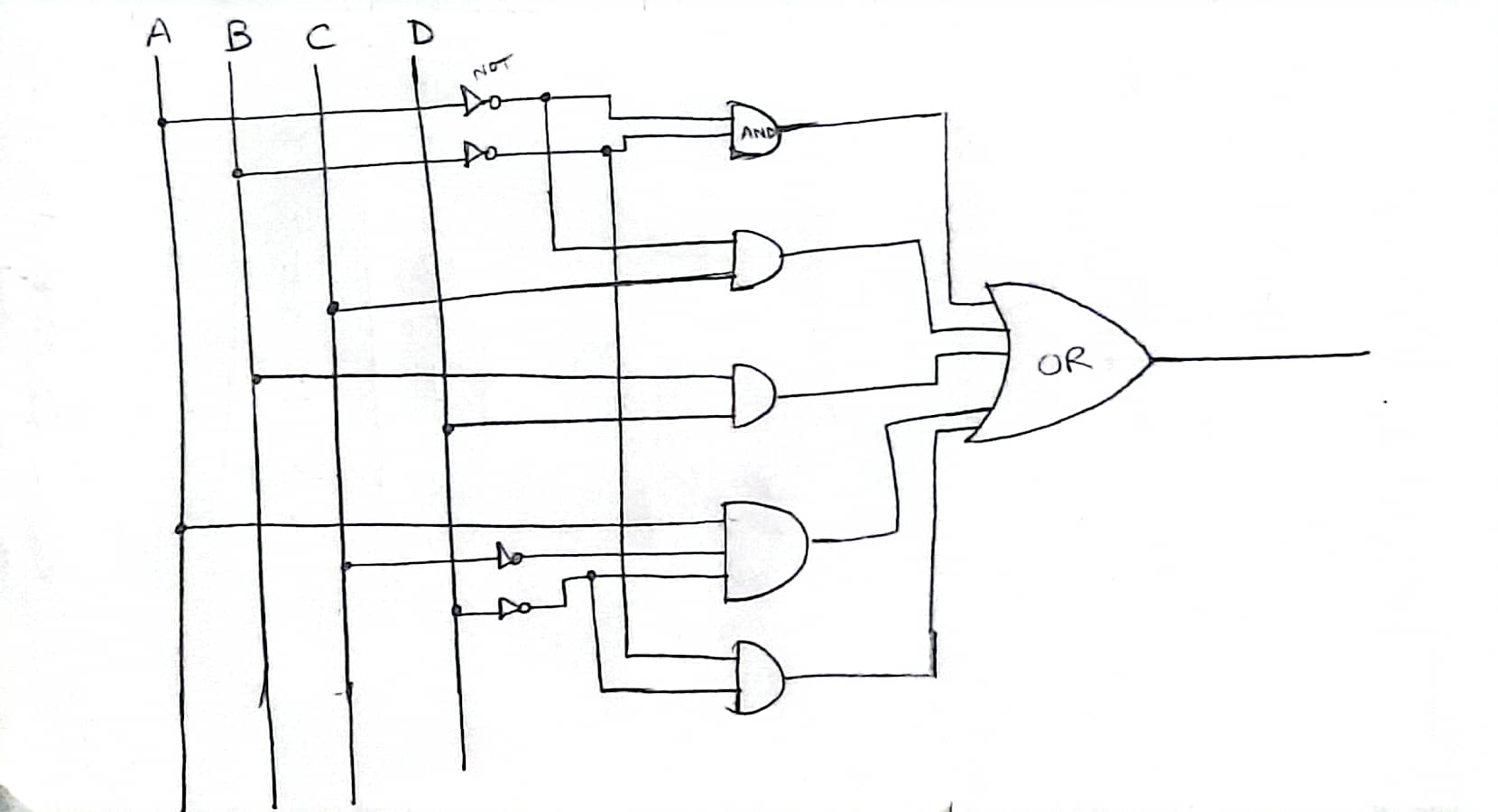
using CMOS technology. You may use blocks/sub-circuits made using CMOS technology but

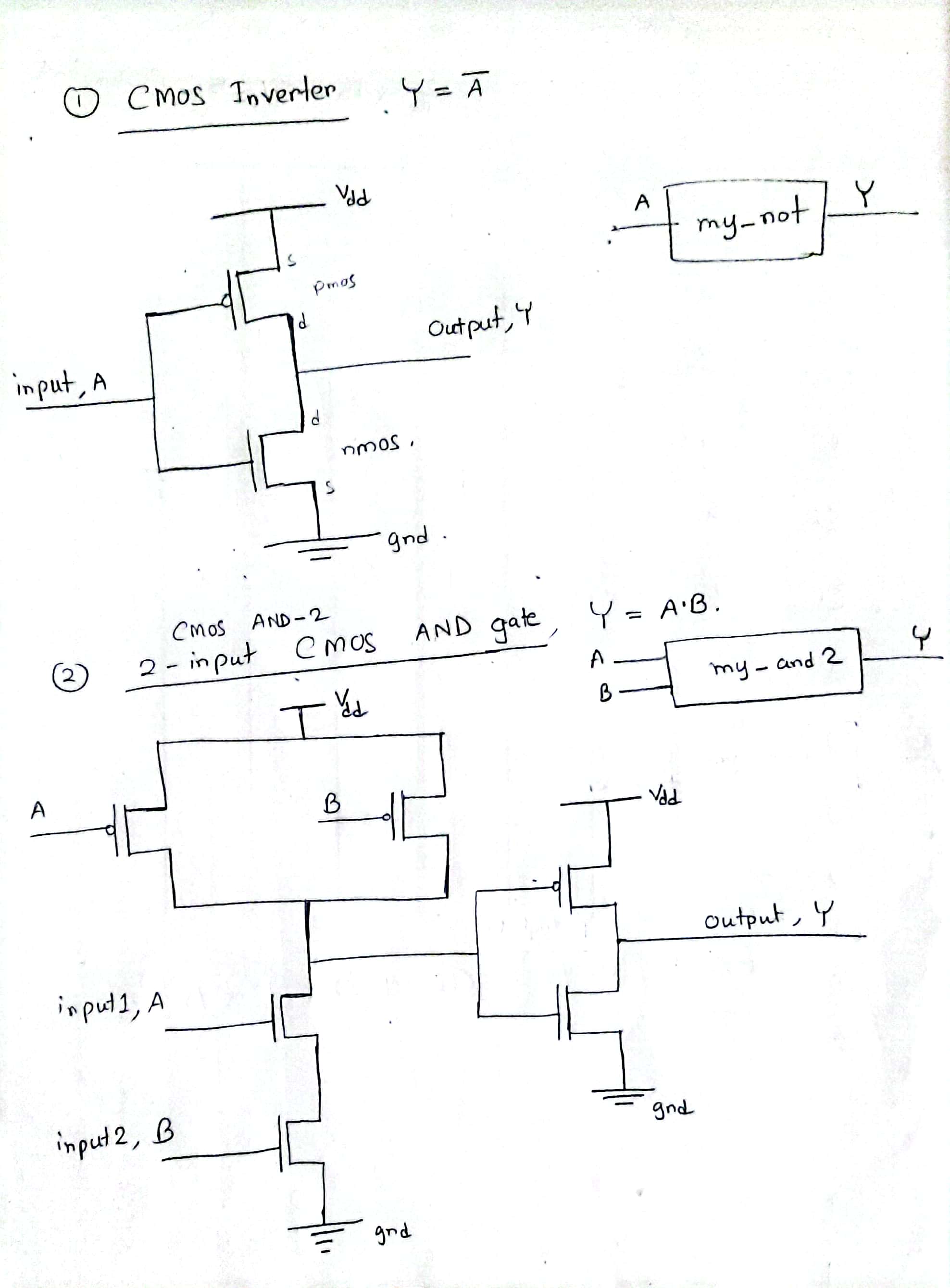
cannot use readily available logic gates.

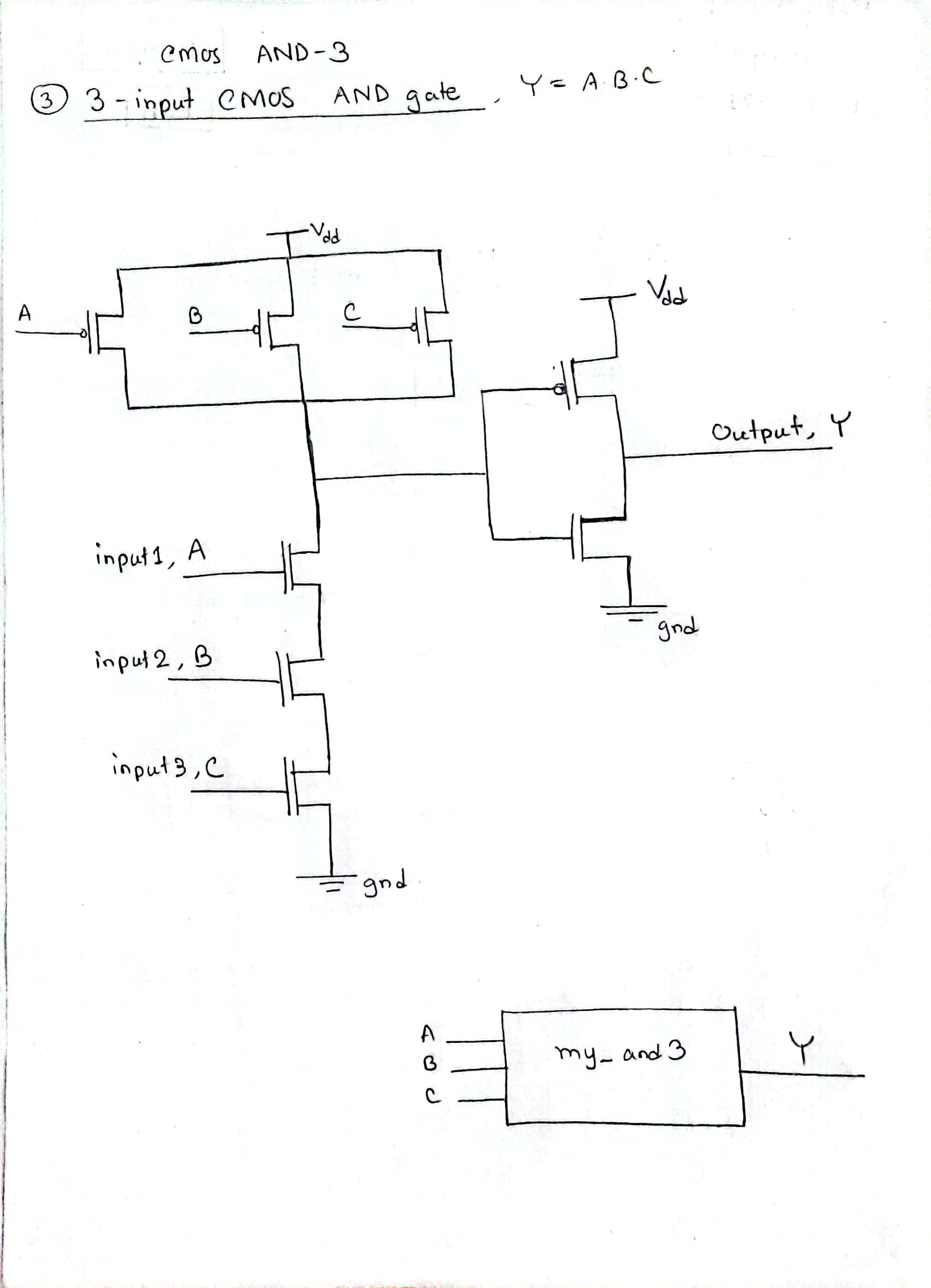


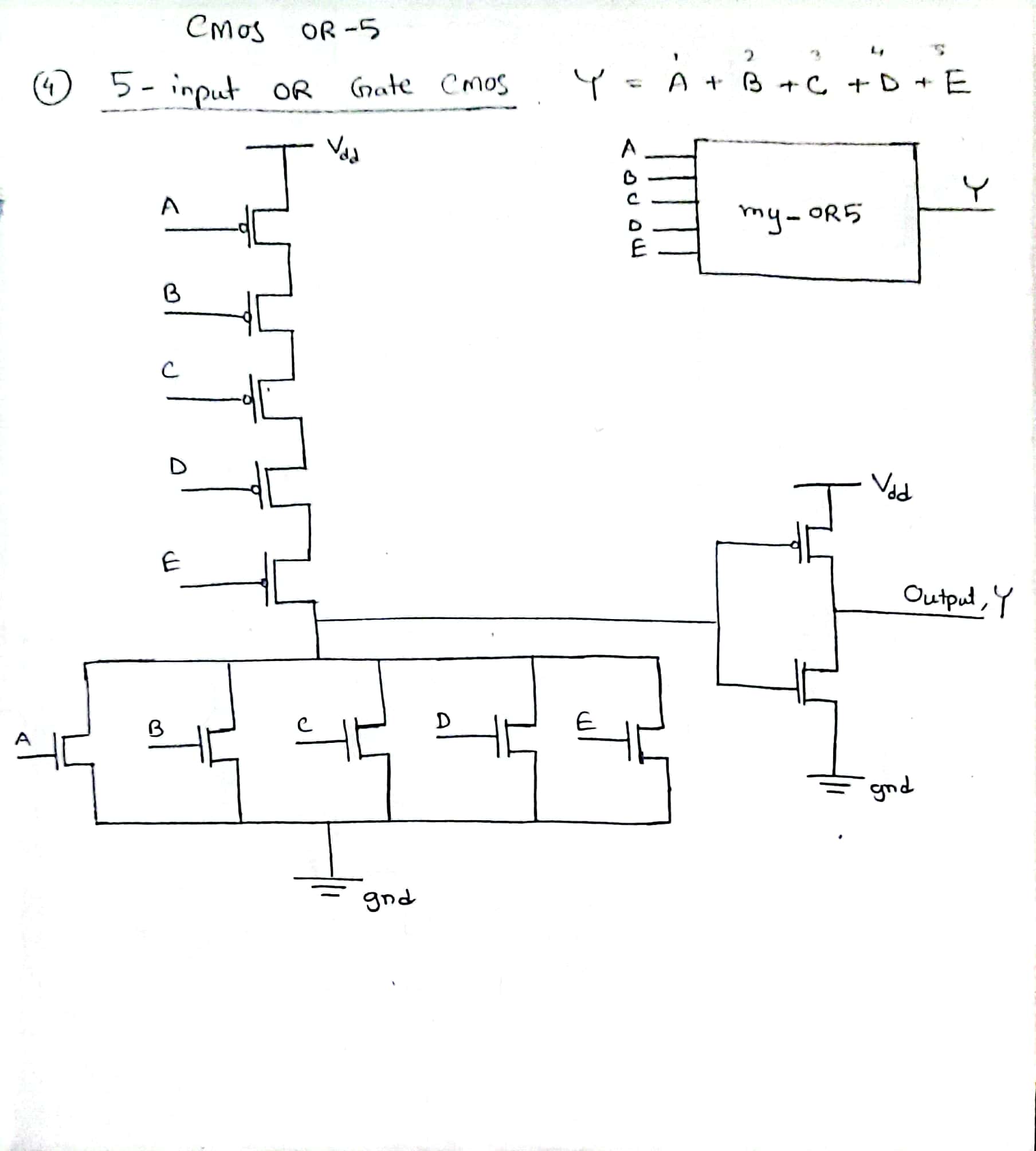
Answer:



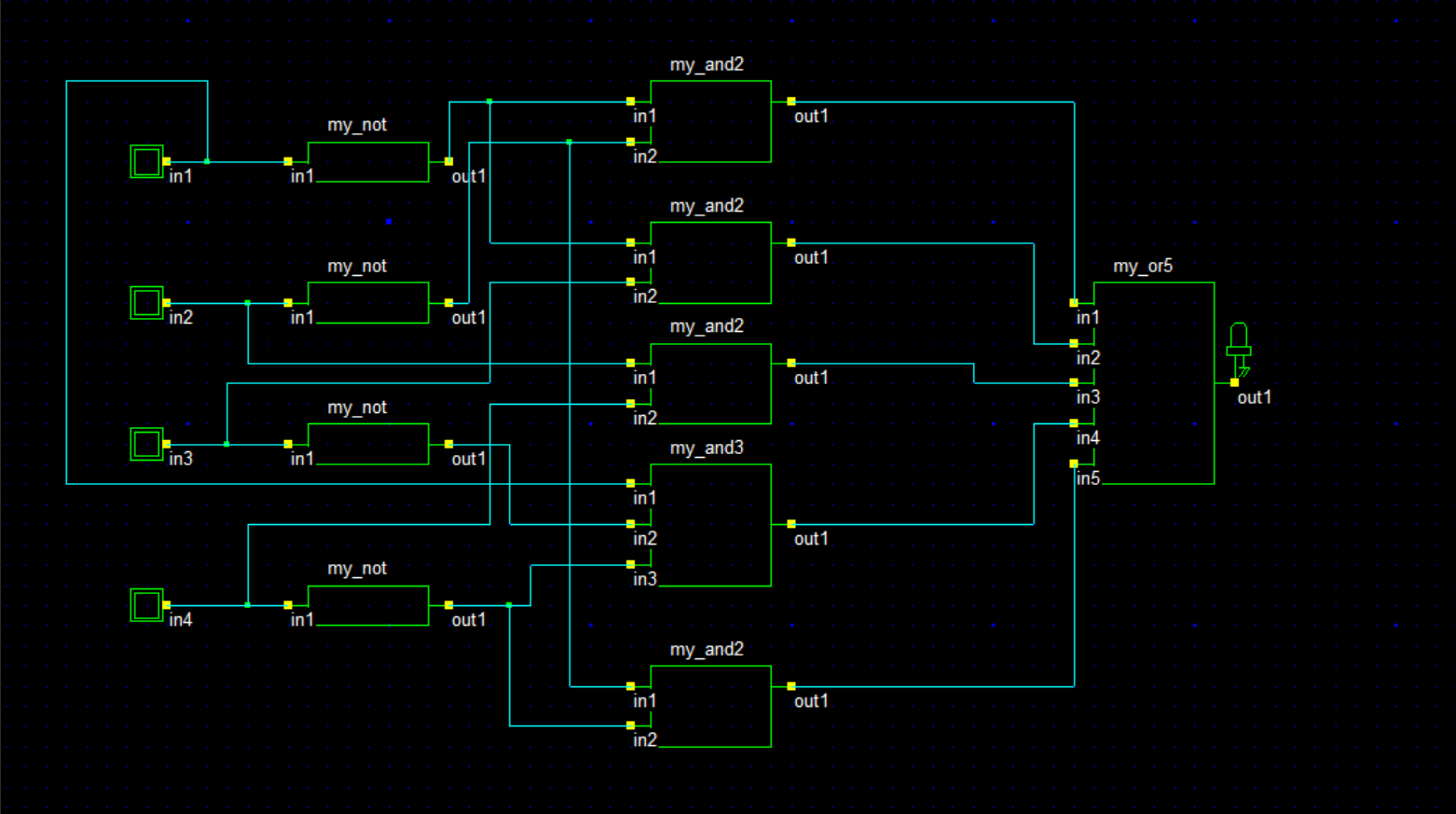




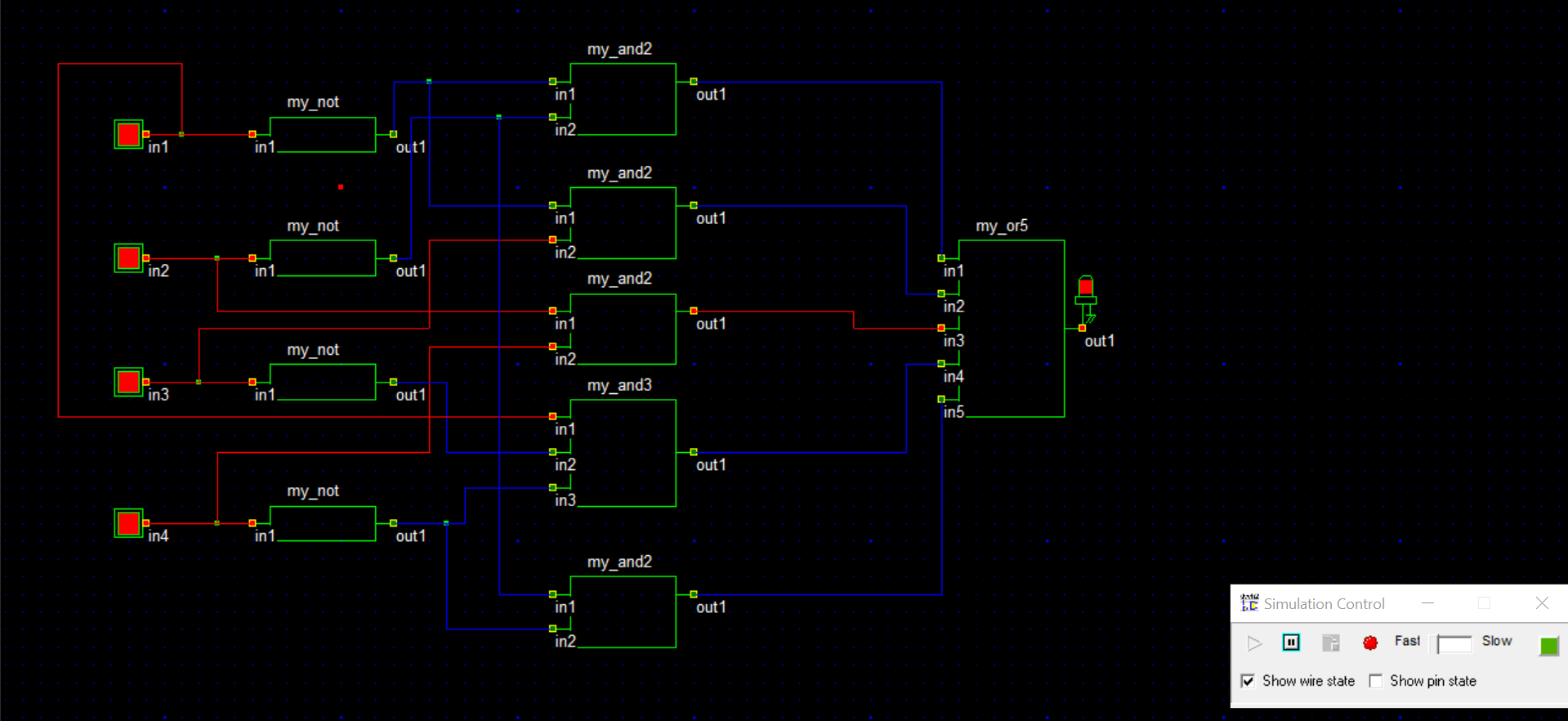




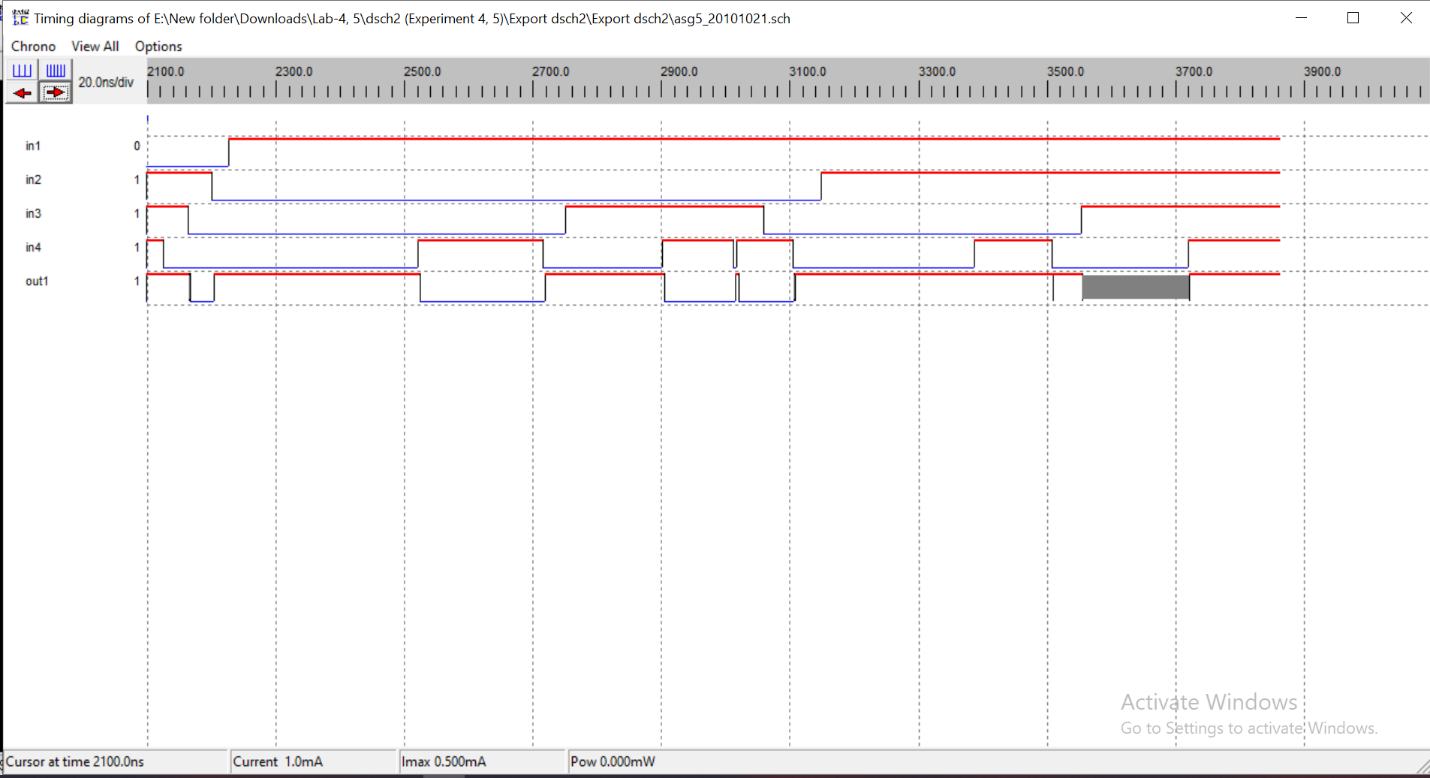
**DSCH2 Design:**



**DSCH2 Simulation:**



**DSCH2 Timing Diagram:**



**Discussion:**

Here, in the Timing Diagram, in1 = A, in2 = B, in3 = C, in4 = D and out1 = Y (or the output).

